CLAIMS

What is claimed is:

1. A method for generating at least one split power plane of a multi-layer printed circuit board (PCB), comprising:

(a) creating a printed circuit board outline;

(b) determining associated locations of a plurality of components within the PCB outline;

(c) creating a power fanout that represents an electrical power distribution to each of the plurality of components, the power fanout supporting a plurality of electrical potentials;

(d) creating a split plane wireframe comprising:

(i) generating a plurality of initial voltage wireframes;

(ii) reducing a quantity of crossover, a crossover corresponding to an intersection of different voltage wireframes; and

(iii) determining a trace width for each segment of the split plane wireframe in accordance with electrical requirements of associated components; and

(e) creating a first split power plane from the split plane wireframe, the first split power plane comprising a first constituent plane associated with a first voltage and a second constituent plane associated with a second voltage.

2. The method of claim 1, wherein (iii) comprises:

(1) calculating the trace width in accordance with electrical current requirements of at least one associated electrical load.

3. The method of claim 2, wherein (iii) further comprises:

(2) if a signal via is situated on a first segment, relocating the signal via.

4. The method of claim 1, wherein (ii) comprises:

(1) if a first crossover exists between a first voltage wireframe and a second voltage wireframe, reconfiguring at least one voltage wireframe to eliminate the first crossover.

5. The method of claim 4, wherein (ii) further comprises:

(2) if another crossover exists between the first voltage wireframe and the second voltage wireframe, reconfiguring the at least one voltage wireframe to eliminate the other crossover.

6. The method of claim 1, wherein a segment is associated with a plurality of electrical loads, and wherein (iii) comprises:

(1) rearranging an ordering of the plurality of electrical loads to reduce a number of vertices of the segment.

7. The method of claim 1, wherein a first electrical load is associated with a segment, and wherein the electrical requirements account for a first peak current requirement of the first electrical load.

8. The method of claim 7, wherein another electrical load is associated with the segment, and wherein the electrical requirements comprise another peak current requirement of the other electrical load, and wherein (iii) comprises:

(1) adding the first peak current requirement to the other peak current requirement to determine the electrical requirements; and

(2) in response to (1), calculating the trace width of the segment.

9. The method of claim 1, wherein a first electrical load is associated with a segment, and wherein the electrical requirements account for a first average current requirement of the first electrical load.

10. The method of claim 9, wherein another electrical load is associated with the segment, and wherein the electrical requirements comprise another average current requirement of the other electrical load, and wherein (iii) comprises:

(1) adding the first average current requirement to the other average current requirement to determine the electrical requirements; and

(2) in response to (1), calculating the trace width of the segment.

11. The method of claim 1, wherein (ii) comprises:

(1) if a crossover exists between a first voltage wireframe and a second voltage wireframe, moving at least one via, wherein the at least one via provides electrical power to one of the plurality of components.

12. The method of claim 1, wherein (ii) comprises:

(1) if the crossover exists between the first voltage wireframe and the second wireframe, moving one of the plurality of the components.

13. The method of claim 1, wherein (ii) comprises:

(1) if the crossover exists between a first voltage wireframe and a second voltage wireframe, routing a segment on a different layer of the multi-layer PCB.

14. The method of claim 1, wherein (d) further comprises:

(iv) reconfiguring the split plane wireframe to avoid at least one impediment, wherein the impediment is selected from the group consisting of a milling path, a route obstruct, a plane obstruct, and a route border.

15. The method of claim 1, wherein (e) comprises:

(i) increasing an area of one of the constituent planes in accordance with the printed circuit board outline.

16. The method of claim 2, wherein (iii) further comprises:

(2) if a via is located on a trace of a segment, adding a vertex to the segment in order to circumvent the via.

17. The method of claim 2, wherein (iii) further comprises:

(2) if a via is located on a trace of the segment, moving a milling path; and

(3) reconfiguring the segment.

18. The method of claim 15, wherein (e) further comprises:

(ii) balancing a first area of the first constituent plane and a second area of the second constituent plane.

19. The method of claim 1, wherein (i) comprises:

(1) connecting a first electrical load with a second electrical load with a wireframe connection selected from the group consisting of a horizontal connection, a vertical connection, and a 45-degree connection.

20. The method of claim 1, further comprising:

(f) repeating (d) and (e) to form another split power plane to support additional electrical potentials.

21. The method of claim 1, wherein at least one of the electrical potentials corresponds to a ground potential.

22. The method of claim 1, further comprising:

(f) creating a second split power plane from the split plane wireframe, wherein the second split power plane resides on a different layer of the multi-layer PCB than does the first split power plane.

23. The method of claim 1, wherein (ii) reduces the quantity of crossovers to zero, thereby eliminating all of the crossovers.

24. A multi-layer printed circuit board having a split power plane designed in accordance with the method of claim 1.

25. A computer-readable medium having computer-executable instructions for performing the method recited in claim 1.

26. A computer-readable medium having computer-executable instructions for performing the method recited in claim 15.

27. An apparatus for routing a split power plane of a multi-layer printed circuit board (PCB), comprising:

an input module;

an output module; and

a processor that is coupled to the input module to obtain circuit requirements and that is coupled to the output module to provide design results for the split power plane, the processor configured to perform:

(a) creating a printed circuit board outline;

(b) determining associated locations of a plurality of components within the PCB outline;

(c) creating a power fanout that represents an electrical power distribution to each of the plurality of components, the power fanout supporting a plurality of electrical potentials;

(d) creating a split plane wireframe comprising:

(i) generating a plurality of initial voltage wireframes;

(ii) reducing a quantity of crossovers, a crossover corresponding to an intersection of different voltage wireframes; and

(iii) determining a trace width for each segment of the split plane wireframe in accordance with electrical requirements of associated components; and

(e) creating a first split power plane from the split plane wireframe, the first split power plane comprising a first constituent plane associated with a first voltage and a second constituent plane associated with a second voltage.

28. The apparatus of claim 27, wherein the processor, whenever performing (iii), is configured to perform:

(1) calculating the trace width in accordance with electrical current requirements of at least one associated electrical load.

29. The apparatus of claim 27, wherein the processor, whenever performing (ii), is configured to perform:

(1) if a first crossover exists between a first voltage wireframe and a second voltage wireframe, reconfiguring at least one voltage wireframe to eliminate the first crossover.

30. The apparatus of claim 27, wherein the processor, whenever performing (e), is configured to perform:

(i) increasing an area of one of the constituent planes in accordance with a printed circuit board outline.

31. The apparatus of claim 27, further comprising:
an input device that enables a user to interact with the apparatus.

32. The apparatus of claim 27, further comprising:
an output device that employs the design results.